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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,118	02/25/2004	Osamu Kimura	1075.1253	1980

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EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,118	KIMURA ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/26/05,2/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statement filed 25 February 2004 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because an English translation of the abstract is not provided for document HEI 7-20994 – line AG of form PTO-1449. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

3. The information disclosure statement (IDS) submitted on 26 August 2005 was fully considered by the examiner. It is worthy to note that the art cited on line AB of form PTO-1449 has an incorrect document number. The correct document number is 2003/0158999.

Drawings

4. The drawings were received on 25 February 2004. These drawings are deemed acceptable for examination.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claims 2-14 and 16-28 are objected to because of the following informalities:

As for claims 2 and 16, the phrase "an page address" (as recited on line 3 of claim 2) should be changed to "a page address".

As for claims 5-8 and 19-22, the phrase "the association" (as recited on line 5 of claim 5) should be changed to "an association".

As for claim 13, the phrase "the association" as recited on lines 16-17, should be changed to "an association".

As for claim 27, the phrase "the entire control unit" as recited on line 9, should be changed to "the entire control apparatus". Additionally, the phrase "the association" as recited on line 23 should be changed to "an association".

As for claims 4 and 18, the phrase "said PCI buses" should be changed to "said PCI bus" to establish antecedent basis.

The remaining claims are objected to for further limiting one of the previously objected to claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "generally" in claims 15 and 27 (as recited on line 9 of claim 15) is a relative term, which renders the claim indefinite. The term "generally" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The claims will further be treated on its merits as if the management modules have at least some control over the control apparatus.

8. Claim 1 recites the limitation "said second module" in line 8. There is insufficient antecedent basis for this limitation in the claim as the claim sets forth more than one second modules previously within the claim. It is assumed that Applicant intended to refer to all of said second modules within this limitation.

9. Claims 5-14 and 19-28 recite the limitation "the second module" and "this second module" in lines 15,19 and 16,20 respectively (of claim 13). There is insufficient antecedent basis for these limitations in the claims. More specifically, it is unclear which of the plurality of second modules as previously set forth, is being referenced in lines 15 and 19 (of claim 13). Furthermore, it is unclear which of the plurality of second modules "this second module" references. Is this the same as "the second module", or the other of the two second modules? It is assumed that "the second module" and "this second module" refers to two different modules. Note the same rejection applies for claims 19-22 and 27 for the "management module" recited in these claims.

10. Claims 9-12, 14, 23-26 and 28 recite the limitation "said cache memory" in line 3 (claim 9), and "the cache memory" in line 5 (claim 9). There is insufficient antecedent basis for these limitations in the claims, as it is unclear which of the plurality of caches is being referenced by these limitations. It is assumed that "said cache memory" refers to the cache memory within the first "second module".

11. Claim 15 recites the limitation "said modules" in lines 15-16. There is insufficient antecedent basis for this limitation in the claim, as it is unclear which, among the first or second modules, is being referenced by the limitation. It is assumed that Applicant intended "said modules" to refer to both the first and second modules.

12. The remaining claims are further rejected for at least inheriting the deficiencies of each of the base claims (1, 13, 15 and 27).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 13-14 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber (US Patent 5,937,174) in further view of Hauck et al. (US PG Publication 2003/0158999 A1), hereinafter Hauck.

As for claims 13 and 27, Weber teaches a storage control apparatus placed between a disk unit and a host for controlling access to said disk unit by said host, said storage control apparatus comprising:

a disk interface module for controlling an interface to said disk unit (Fig. 2, element 138.1);

a host interface module for controlling an interface to said host (Fig. 2, element 204);

Though Weber teaches multiple management modules (disks (106) within the disk storage system (104)), he fails to teach said modules containing cache used to mirror data.

Hauck however teaches an apparatus for maintaining cache coherency in a storage system, which includes a storage system (Fig. 1, elements 110, 112 ... 118, 120, 130 and 160) including a plurality of control units (Fig. 1, element 110, 112, ...

118). Referring to Fig. 2, each control unit (i.e. controller) contains a Read Write Cache Area, and a Cache Copy Area – paragraph 0039, all lines. Since Hauck's controllers inherently controller access to the storage system, they assert at least some control over the control system.

Weber further teaches:

> a bridge module connected through an interface bus to said disk interface module, said host interface module and said management modules for making connections among said disk interface module (Fig. 2, element 206),
>
> said host interface module and said management modules for data transfer among said modules, said host interface module writing data to be written, which is received from said host, through said bridge module into cache memories of two of said plurality of management modules (referring again to Fig. 2, the host can communicate with the storage module (element 104, which contains multiple modules or drives) via the host interface, the bridge and the disk interfaces (elements 204, 206, and 138.1 respectively)) - col. 7, line 47 through col. 8, lines 39. It is worthy to note that even though Weber teaches storing in the disks rather than the cache, an obvious variation of Weber's apparatus would include Hauck's storage system, as will be discussed *infra*.

Again, Weber fails to teach the management modules as containing cache with the ability to mirror data, however Hauck teaches each of said management modules including management means (each controller is used to manage read/write functions to the cache) for managing information on the management module which is in mirror relation to this management module (referring to Fig. 2, Host Write #1 data (230) is

written to controller 2 (i.e. mirrored), and likewise Host Write #2 data (270) is mirrored to controller 1 – paragraph 0039-0040 all lines). Hauck additionally teaches managing the association between a master area address in said cache memory in this management module and a mirror area address in said cache memory of the management module being in the mirror relation to this management module (referring to Fig. 4, a master area for each cache is maintained (Read/Write/Copy Cache)). The controllers maintain cache coherency by transmitting and receiving metadata, which comprise a bit map and cache identifier. These data allows the controllers to maintain their respective hash tables (Fig. 4, elements 490 and 495) which allows the controllers to maintain where cache lines are present in the cache area, and also maintain a free list of mirror locations (paragraphs 0045-0048, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

As for claims 14 and 28, Hauck teaches a case in which a capacity of a master area of said cache memory runs short when data read out from said disk unit through

said disk interface module and said bridge module is temporarily preserved in the cache memory, each of said management modules preserves the readout data in a mirror area of said cache memory of the management module, which is in the mirror relation to this management module, on the basis of a situation of management by said management means (Hauck discusses the system's ability to preserve data by reading out the data from a survivor controller (referring to Fig. 7, element 710) and reading into a replacement controller (730) to preserve data that was stored in the failed controller (720). This process takes place in case of a controller failure, or if a large ownership of data is shouldered by the controller (i.e. cache becomes full) – paragraph 0054-0056, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

14. Claims 1-12 and 15-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Weber (US Patent 5,937,174) and Hauck

(US PG Publication 2003/0158999 A1), and in further view of Hashimoto et al. (US PG Publication 2002/0016898 A1), hereinafter Hashimoto.

As for claims 1, and 15, Weber teaches a storage control apparatus placed between a disk unit and a host for controlling access to said disk unit by said host, said storage control apparatus comprising:

a disk interface module for controlling an interface to said disk unit (Fig. 2, element 138.1);

a host interface module for controlling an interface to said host (Fig. 2, element 204);

Though Weber teaches multiple management modules (disks (106) within the disk storage system (104)), he fails to teach said modules containing cache used to mirror data.

Hauck however teaches an apparatus for maintaining cache coherency in a storage system, which includes a storage system (Fig. 1, elements 110, 112 ... 118, 120, 130 and 160) including a plurality of control units (Fig. 1, element 110, 112, ... 118). Referring to Fig. 2, each control unit (i.e. controller) contains a cache area (270), and a cache copy area (280) – paragraph 0039, all lines. Since Hauck's controllers inherently controller access to the storage system, they assert at least some control over the control system.

Weber further teaches:

a bridge module connected through an interface bus to said disk interface module, said host interface module and said management modules for making

connections among said disk interface module, said host interface module and said management modules for data transfer among said modules (Fig. 2, element 206),

said bridge module including:

address production means for analyzing said addressing information, which is received together with said data to be written from said host interface module, to produce two transferred-to addresses for designation of said two management modules having said cache memories in which said data is to be actually written and to produce written-in addresses in said cache memories (col. 8, lines 20-39) – the bridge unit works in conjunction with the host interface and the memory controller. The bridge unit receives data and address from the host interface and memory controller in order to communicate with (i.e. perform memory access functions on) the memory subsystem. The interface and memory controller help to permit the bridge to get the correct data to the correct locations on the disks within the subsystem; and

data transfer control means for controlling data transfer from said bridge module to said management modules so that, after said data is transferred to the two management modules corresponding to said two transferred-to addresses, said data is written at said written-in address in said cache memory of each of the two management modules (Fig. 2, the host (108) can write and read data to and from the storage system via the host interface (204) to the bridge (206), through the device interface (138.1) – col. 7, line 47 through col. 8, lines 39).

Again, it is worthy to note that even though Weber teaches storing in the disks rather than the cache, an obvious variation of Weber's apparatus would include Hauck's storage system, as per the discussion *supra* (per claims 13 and 27). When the host writes to the storage system, the data is mirrored in Hauck's system such that at least two addresses (one for each controller's cache) are written-in to.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

Neither Weber nor Hauck teach the host interface as generating the address to select where data is to be written.

Hashimoto however teaches a host interface circuit in which a host interface device (Fig. 3, element 103) has the ability to generate two unique address via the address generating circuit (206a), which uses two pointers to help generate the addresses (paragraph 0064, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further incorporate Hashimoto's host interface device into his own memory structure for high data bandwidth RAID applications. By doing so, Weber would have a more efficient means of interfacing from his host to bridge unit, which includes reducing the power consumption caused by excessive signal transition on the address bus as taught by Hashimoto in paragraphs 0013 and 0017, all lines.

As for claims 2-3 and 16-17, Hashimoto further teaches designating, in said addressing information, a page address in said cache memory of each of said management modules and an offset address in a page designated by said page address, as said written-in address for said data in said cache memory, and specific information for specifying said two management modules having said cache memories in which said data is to be actually written, as said two transferred-to addresses for said data (Hashimoto discusses address conversion circuitry for both the first and second addresses. The address conversion circuitry uses the generated address and an offset (inherent for the conversion to take place) to generate appropriate addresses, in order to access the memories, paragraph 0019-0020, all lines).

As for claims 4 and 18, Weber teaches interface bus is a PCI (Peripheral Component Interconnect) bus, and numbers for specifying said PCI bus for said two management modules are designated as said specific information (col. 8, lines 20-39). It is worthy to note that since Weber only teaches one bus line, the addresses generated by Hashimoto could only refer to the one address bus that is used to transfer the data specified by the generated addresses.

Again, it would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further incorporate Hashimoto's host interface device into his own memory structure for high data bandwidth RAID applications. By doing so, Weber would have a more efficient means of interfacing from his host to bridge unit, which includes reducing the power consumption caused by excessive signal transition on the address bus as taught by Hashimoto in paragraphs 0013 and 0017, all lines.

As for claims 5-8 and 19-22, Weber teaches each of said management modules includes management means for managing information on the management module which is in mirror relation to this management module and for managing the association between a master area address in said cache memory in this management module and a mirror area address in said cache memory of the management module being in the mirror relation to this management module referring to Fig. 2, host write 1 data (230) is written to controller 2 (i.e. mirrored), and likewise host write data 2 (270) is mirrored to controller 1 – paragraph 0039-0040 all lines. Additionally, Weber teaches (referring to Fig. 4) a master area for each cache is maintained (Read/Write/Copy Cache). The controllers maintain cache coherency by transmitting and receiving metadata, which comprise a bit map and cache identifier. These data allows the controllers to maintain their respective hash tables (Fig. 4, elements 490 and 495) which allows the controllers to maintain where cache lines are present in the cache area, and also maintain a free list of mirror locations (paragraphs 0045-0048, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache

coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

Hashimoto teaches address designation means of said host interface module produces said addressing information on the basis of information acquired from said management means of one of the two management modules (Fig. 3, element 103) has the ability to generate two unique address via the address generating circuit (206a), which uses two pointers to help generate the address (paragraph 0064, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further incorporate Hashimoto's host interface device into his own memory structure for high data bandwidth RAID applications. By doing so, Weber would have a more efficient means of interfacing from his host to bridge unit, which includes reducing the power consumption caused by excessive signal transition on the address bus as taught by Hashimoto in paragraphs 0013 and 0017, all lines.

As for claims 9-12 and 23-26, Hauck teaches a case in which a capacity of a master area of said cache memory runs short when data read out from said disk unit through said disk interface module and said bridge module is temporarily preserved in the cache memory, each of said management modules preserves the readout data in a

mirror area of said cache memory of the management module, which is in the mirror relation to this management module, on the basis of a situation of management by said management means (Hauck discusses the system's ability to preserve data by reading out the data from a survivor controller (referring to Fig. 7, element 710) and reading into a replacement controller (730) to preserve data that was stored in the failed controller (720). This process takes place in case of a controller failure, or if a large ownership of data is shouldered by the controller (i.e. cache becomes full) – paragraph 0054-0056, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tanaka et al. (US Patent 6,502,167 B1) teach a duplicated shard memory controller for disk array.

Hauck et al. (US Patent 6,807,611 B2) teach high speed selective mirroring of cache data.

Sicola et al. (US Patent 6,279,078 B1) teach an apparatus for a dual cache memory system operating in a plurality of cache modes.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

Mano Padmanabhan 3/14/06
MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER